REMARKS

Claims 1-6, 8-13 and 15-20 are in the application. Claims 7 and 14 have been cancelled previously.

Response to 35 U.S.C. §102 Rejections

Claims 1-6, 8-13, and 15-20 were rejected under 35 U.S.C. §102 as being anticipated by Blanchard, USP 6,686,244. This rejection is respectfully traversed in view the remarks presented hereinafter.

Claim 1 calls for a method of making a semiconductor vertical trench gate junction FET device including the steps of providing a body of semiconductor material comprising a first conductivity type, wherein the body of semiconductor material has an upper surface and a lower surface opposing the upper surface, wherein the lower surface provides a drain contact. The method also calls for forming a first trench in the body of semiconductor material and extending from the upper surface, wherein the first trench has a first width, a first depth from the upper surface, first sidewalls, and a first bottom surface. The method additionally calls for forming a second trench within the first trench, wherein the second trench has a second width, a second depth from the first surface, second sidewalls and a second bottom surface. The method further calls for forming a first source region in the body of semiconductor material extending from the upper surface and spaced apart from the first trench by a portion of the body of semiconductor material. The method still further calls for introducing a dopant of a second conductivity type into at

least a portion of the second sidewalls and the second bottom surface to form a doped trench gate region, wherein the doped trench gate region extends into the body of semiconductor material for controlling conduction in the device. Moreover, the method calls for forming a first passivation layer over the doped trench gate region, and forming a second passivation layer over the first passivation layer thereby filling at least the second trench.

Applicant respectfully submits that the Blanchard fails to anticipate claim 1 for at least the following reasons. First, claim 1 calls for a method of making a trench gate JFET device. As is evident in FIG. 4 of Blanchard, Blanchard's structure is clearly a planer gate device (see element 418 and OXIDE). Regions 440 and 442 are not gate regions at all, but are instead p-type continuous columns (see column 4, lines 30-53), which help improve breakdown voltage. These regions have absolutely nothing to do with gate or current control. Moreover, claim 1 calls for forming a JFET device, Blanchard specifically teaches forming a MOSFET device. Thus, for at least these reasons, applicant respectfully submits that Blanchard fails to anticipate claim 1.

Claims 2-6, and 8-11 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 12 calls for a process for making a compound semiconductor vertical trench gate junction FET device comprising the steps of forming a first groove in a compound semiconductor layer of a first conductivity type, wherein the first groove has first sidewalls and a first lower surface, and wherein the first groove extends from a first

surface of the compound semiconductor layer. The process also calls for forming a second groove within the first groove, wherein the second groove has second sidewalls and a second lower surface. In addition, the process includes doping the second lower surface and at least a portion of the second sidewalls with a second conductivity type dopant to form a doped trench gate region in the compound semiconductor layer, and forming a first source region of the first conductivity type in the compound semiconductor layer adjacent to the first groove. Additionally, the process includes forming a source contact to the first source region, and filling the second groove and at least a portion of the first groove with a passivation layer. Further, the process calls for forming a gate contact coupled to the doped trench gate region, and forming a drain contact on a second surface of the compound semiconductor layer.

Applicant respectfully submits that the Blanchard fails to anticipate claim 12 for at least the following reasons. First, claim 12 calls for a method of forming a doped trench gate region in a compound semiconductor layer for controlling conduction in the device. As is evident in FIG. 4 of Blanchard, Blanchard's structure is clearly a planer gate device (see element 418 and OXIDE). Regions 440 and 442 are not gate regions at all, but are instead p-type continuous columns (see column 4, lines 30-53), which help improve breakdown voltage. These regions have absolutely nothing to do with gate or current control. Moreover, claim 12 calls for forming a JFET device, Blanchard specifically teaches a MOSFET device. Further, claim 12 calls for forming a first groove in a compound semiconductor layer. Blanchard only teaches a silicon layer, not a compound

semiconductor layer (see column 4, lines 30-34). Thus, for at least these reasons, applicant respectfully submits that Blanchard fails to anticipate claim 12.

Claims 13 & 15-17 depend from claim 12 and are believed allowable for at least the same reasons as claim 12.

Claim 18 calls for a method for forming a compound semiconductor trench gate junction FET device comprising the steps of providing a body of compound semiconductor material including a support wafer of a first conductivity type and a first dopant level and an epitaxial layer formed over the support wafer, wherein the epitaxial layer is of the first conductivity type and has a second dopant level lower than the first dopant level. The method also calls for forming a plurality of spaced apart first doped regions of the first conductivity type in the epitaxial layer, and forming a plurality of first trenches in the epitaxial layer, wherein each first trench is between a pair of first doped regions. Additionally, the method calls for forming a plurality of second trenches in the epitaxial layer, wherein one second trench is within one first trench, and doping at least portions of sidewall surfaces and lower surfaces of each second trench to form a plurality of doped trench gate regions, wherein the plurality of doped gate regions extend into the body of compound semiconductor material. Moreover, the method calls for filling the plurality of second trenches and at least a portion of the plurality of first trenches with a passivation material. In addition, the method calls for coupling the plurality of spaced apart first doped regions with a first contact layer, and coupling the plurality of doped trench gate regions to a gate connecting region formed in the body of compound

semiconductor material. Further, the method calls for forming a drain contact on a second surface of the support wafer.

Applicant respectfully submits that the Blanchard fails to anticipate claim 18 for at least the following reasons. First, claim 18 calls for a method of forming a plurality of doped trench gate regions in a compound semiconductor layer that are configured for controlling conduction in the device. As is evident in FIG. 4 of Blanchard, Blanchard's structure is clearly a planer gate device (see element 418 and OXIDE). Regions 440 and 442 are not gate regions at all, but are instead p-type continuous columns (see column 4, lines 30-53), which help improve breakdown voltage. These regions have absolutely nothing to do with gate or current control. Further, claim 18 calls for forming a JFET device, Blanchard specifically teaches a MOSFET device. Moreover, claim 18 calls for providing a body of compound semiconductor material. Blanchard only teaches a silicon, not a compound semiconductor material (see column 4, lines 30-34). Thus, for at least these reasons, applicant respectfully submits that Blanchard fails to anticipate claim 18.

Claims 19 and 20 depend from claim 18 and are believed allowable for at least the same reasons as claim 18.

In view of all of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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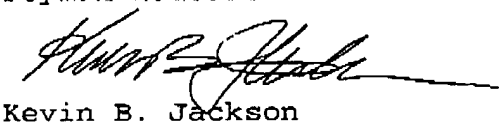

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